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Abstract of the Disclosure

An integrated circuit thin film capacitor includes multiple layers of conductors separated by dielectric material. The conductive layers are connected to interconnect lands using conductive vias. The interconnect lands can be controlled collapse chip connection (C4) lands that allow the capacitor to be connected to a circuit board. In one embodiment, the capacitor is mounted on a circuit board in close proximity to a processor circuit. The multi layer capacitor of the present invention provides the ability to increase a capacitance value while lowering interconnect resistance and inductance.

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